REMARKS:

Claims 1, 3, 4, and 8-16 are currently pending. Claims 1, 3, 4, and 8-11 are currently being considered, of which claims 1 and 11 have been amended herein. Claims 12-16 have been withdrawn from consideration. Claims 2 and 5-7 have been canceled herein without prejudice or disclaimer as to their subject matter. The Examiner has indicated that claims 2, 8, and 10 set forth allowable subject matter.

The Examiner has rejected claims 5-7 under the first paragraph of 35 USC 112.

The rejection of claims 5-7 is moot and should be withdrawn, because claims 5-7 have been canceled herein without prejudice or disclaimer as to their subject matter.

The Examiner has rejected claims 1, 3, 4 and 9 under 35 USC 102(e) as anticipated by USP 6,720,589 (**Shields**).

Applicant respectfully traverses this rejection, for the following reasons.

Shields fails to expressly or inherently describe the following features set forth in claim 1, as amended: "the dot-shaped structure is caused to form on the surface of the second semiconductor layer at a position above the quantum dot due to crystal strains generated in the surface of the second

semiconductor layer due to the presence of the quantum dot," in combination with the other claimed features.

Accordingly, Applicant respectfully submits that this rejection of claim 1 should be withdrawn. It is submitted that this rejection of claims 3, 4, and 9 should be withdrawn by virtue of their dependency.

The Examiner has rejected claim 11 under 35 USC 102(b) as anticipated by USP 6,498,360 **(Jain et al.)**.

Applicant respectfully traverses this rejection, for the following reasons.

Jain et al. disclose a modulation-doped field-effect transistor comprising: an electron gas layer 19 formed over a substrate 10, and a not-intentionally-doped well 20. The not-intentionally-doped well 20 has two SiGe coupled sub-wells 23, 25 separated via a thin Si barrier layer 24. A channel region is defined by insulation regions 21, 22 buried in a cap layer 18, the not-intentionally-doped well 20 and a first p-doped layer 11. Source/drain implantation layers 16 are formed on both sides of the channel region (see FIG. 9).

However, the features disclosed by the subject application are different from the features of **Jain et al.**

First, in the subject application, a dot-shaped structure 24 is formed on the surface of the second semiconductor layer 22 at a position above the quantum dot 20 due to strains generated in the surface of the second semiconductor layer 22 due to the presence of the quantum dot 20 (see FIG. 1 of the subject application).

Jain et al. do not describe, teach, or suggest such features of the subject application.

Second, in the subject application, oxide layers 26a, 26b are formed on the upper surface of the second semiconductor layer 22 on both sides of the dot-shaped structure 24 with the dot-shaped structure 24 as a mark.

Jain et al. do not describe, teach, or suggest such oxide layers.

Third, in the subject application, depletion regions 28a, 28b are formed in regions of the first semiconductor layer 18 below the oxide layers 26a, 26b, and a channel region 29 is defined by the depletion regions 28a, 28b.

Jain et al. do not describe, teach, or suggest such depletion regions.

Fourth, in the subject application, a gate electrode 32 is electrically connected to the dot-shaped structure 24.

In **Jain et al.** a gate electrode 17 is not electrically connected to a quantum dot (see FIGs. 2(a), 8, and 9).

In the subject application, the dot-shaped structure 24 is formed on the surface of the second semiconductor layer 22 at the position above the quantum dot 20 due to strains generated in the surface of the second semiconductor layer 22 due to the presence of the quantum dot 20. Therefore, the dot-shaped structure 24 is formed on the surface of the semiconductor layer 22 at the position accurately above the quantum dot 20, even in a case that the quantum dot 20 is buried in the semiconductor layer 22. Therefore, in the subject application, it is possible to access to the quantum dot 20 accurately. Accordingly, with the features of the subject application, it is possible to provide a single electron transistor with high performance without failure.

Jain et al. do not describe, teach, or suggest such feature of the subject application.

Jain et al. fail to expressly or inherently describe the following features set forth in claim 11, as amended: "forming oxide layers on the upper surface of the second semiconductor layer on both side of the dot-shaped structure with the dot-shaped structure as a mark to thereby form depletion regions in regions of the first semiconductor layer below the oxide layers, and define a channel region by the depletion regions; forming source/drain regions connected to both ends of the channel region in the second semiconductor layer; and forming a gate electrode electrically connected to the dot-shaped structure," in combination with the other claimed features.

Accordingly, Applicant respectfully submits that this rejection of claim 11 should be withdrawn.

The Examiner has indicated that claims 2, 8, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant appreciates this indication of allowable subject matter, and respectfully requests that the Examiner hold this objection in abeyance while considering the remarks herein regarding base claim 1.

In view of the aforementioned amendments and accompanying remarks, it is respectfully submitted that all claims currently being considered are in condition for examination.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due now or in future with respect to this application, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
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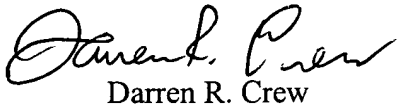

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Enclosure: Petition for Extension of Time